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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,753	09/30/2004	Taizo Yamawaki	843.44318X00	8311

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EXAMINER

CHEN, JUNPENG

ART UNIT	PAPER NUMBER
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2631

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/509,753

Applicant(s)

YAMAWAKI ET AL.

Examiner

Junpeng Chen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 371 and 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Information Disclosure Statement***

2. The information disclosure statement submitted on September 30, 2004 has been considered by the Examiner and made of record in the application file.

***Objection - Drawing***

3. The drawings are objected to because some figures have blocks that lack descriptive labels. For example, block 300 in figure 1 should be additionally labeled as: "base band circuit". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date

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of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 150 in Fig. 1. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "voltage Vcc" in page 20 line 3. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is

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being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Appropriate correction is required.

#### ***Objection - Specification***

4. The disclosure is objected to because of the following informalities:
  - a) On **page 13 line 18**, replace "appreciate" with --appropriate--.
  - b) On **page 14 line 4**, replace "signals frequency-divided" with --frequency-divided signals--.
  - c) On **page 37 line 14**, replace "rage" with --range--.

Appropriate correction is required.

#### ***Objection - Claims***

5. Claims 1, 2, and 5 are objected to because of the following informalities:
  - a) On **line 8 of claim 1**, replace "and" with --for--.
  - b) On **line 17 of claim 2**, replace "and" with --for--.
  - c) On **line 5 of claim 5**, replace "filer" with --filter--.

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

**Claims 1-2, 6, 7 and 10** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Consider **claim 1**, the phrase “current-output type” renders the claims indefinite because the addition of the word “type” to an otherwise definite expression (e.g., current-output) extends the scope of the expression so as to render it indefinite (*Ex parte Copenhaver*, 109 USPQ 118 (Bd. App. 1955)). See MPEP § 2173.05(b).

Consider **claim 2**, the phrases “perfect integrator type” and “current-output type” render the claim indefinite because the addition of the word “type” to an otherwise definite expression (e.g., perfect integrator) extends the scope of the expression so as to render it indefinite (*Ex parte Copenhaver*, 109 USPQ 118 (Bd. App. 1955)). See MPEP § 2173.05(b).

Consider **Claim 6** recites the limitation “said amplitude detector” in both lines 4 and 6 of claim 6. There is insufficient antecedent basis for this limitation in the claim.

Consider **Claim 7** recites the limitation “said first and second operating modes” in lines 3-4 of claim 7. There is insufficient antecedent basis for this limitation in the claim.

Consider **Claim 10** recites the limitations “said first automatic gain controlled amplifier” and “said second automatic gain controlled amplifier” in lines 3-5 of claim 10. There is insufficient antecedent basis for these two limitations in the claim.

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***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claims 1, 2, 6-7 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Midtgaard et al. (U.S. PGPub 2002/0090921 A1)** in view of **Tachimori (U.S. PGPub 2002/0051508 A1)**.

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Consider **claim 1**, Midegaard et al. discloses a transmitter comprising:

a phase control loop (read as the phase path which comprises voltage controlled oscillator 41, power amplifier 33, mixer 44, low pass filter 45, limiters 37 and 38, phase detector 39 and Loop filter 40, paragraph [0048], Fig. 5), for controlling a phase of a carrier being output from a transmission oscillator (read as voltage controlled oscillator 41, (paragraphs [0046] to [0048]), Fig. 5); and

an amplitude control loop (read as the amplitude path which comprises power amplifier 33, mixer 44, low pass filter 45, envelope detectors 27 and 28, comparator 29, loop filter 30 and envelope controller 31, paragraph [0048], Fig. 5) for controlling an amplitude of a transmission being output signal output from a power amplifier (read as the power amplifier 33, (paragraphs [0046] to [0048]), Fig. 5)

However, although Midegaard et al. discloses a current-output circuit (the circuit combination of envelope detectors 27 and 28 and comparator 29, Fig. 5) in the front stage of the filter (loop filter 30, Fig. 5) and discloses that this filter could be Type II filter with two poles (paragraph [0049]), Midegaard et al. failed to specifically disclose that wherein the filter provided on the amplitude control loop (the examiner interprets this filter as a loop filter inside a control loop) for restricting a frequency band of said amplitude control loop is configured by a first passive filter including a capacitor and a resistor and a second passive filter including only a capacitor, and current-output type circuit are provided at the respective front stages of said first passive filter and said second passive filter.



In related art, Tachimori discloses a loop filter in a control loop, which comprises filter 3 and filter 4 (paragraph [0164], Fig. 1). The examiner notices that filter 4 includes a resistor RLP and capacitor CLP. However, it is well known in the art that even without the resistor RLP (current-output type circuit), capacitor CLP itself that is being connected to the ground line would still perform as a low pass filter. Thus, the examiner interprets that resistor RF1 in series connection with capacitor CF1 is a first passive filter with lag-lead characteristic and capacitor CLP itself being connected to the ground line is a second passive filter, which including ONLY one capacitor. Also, resistor RLP is interpreted as a current-output circuits at the front stage of the second passive filter.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of Tachimori on loop filter into the teachings of Midgaard et al. for the purpose of being able to easily adjust the parameter values to meet the desired performance of the transmitter.

Consider **claim 2**, Midgaard et al. discloses a transmitter comprising:

a transmission oscillator (read as voltage controlled oscillator 41, Fig. 5) for generating a carrier (read as the output of voltage controlled oscillator 41);

a power amplifier (read as the power amplifier 33, Fig. 5) for amplifying a generated carrier signal;

a phase control loop (read as the phase path which comprises voltage controlled oscillator 41, power amplifier 33, mixer 44, low pass filter 45, limiters 37 and 38, phase detector 39 and Loop filter 40, paragraph [0048], Fig. 5) which includes a phase detector (read as the circuit of limiters 37 and 38 in connection with phase detector 39)

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for comparing a reference signal (read as RF Input, Fig. 5) and a feedback signal (read as the signal from low pass filter 45) and for outputting a signal corresponding to a phase difference thereof, and which controls a phase of the carrier being output from a transmission oscillator (paragraphs [0046] to [0048]); and

an amplitude control loop (read as the amplitude path which comprises power amplifier 33, mixer 44, low pass filter 45, envelop detectors 27 and 28, comparator 29, loop filter 30 and envelope controller 31, paragraph [0048], Fig. 5) which includes an amplitude detector (envelop detectors 27 and 28 in connection with comparator 29) for comparing a reference signal (read as RF Input, Fig. 5) and a feedback signal (read as the signal from low pass filter 45) and for outputting a signal corresponding to an amplitude difference thereof, and which controls an amplitude of a transmission being output signal output from a power amplifier (paragraphs [0046] to [0048])

However, although Midegaard et al. discloses a current-output circuit (read as a amplitude detector, which comprises envelope detectors 27, 28 and comparator 29, Fig. 5) in the front stage of the filter (loop filter 30, Fig. 5) and discloses that this filter could be Type II filter with two poles (paragraph [0029]), Midegaard et al. failed to specifically disclose that wherein the filter provided on the amplitude control loop (the examiner interprets this filter as a loop filter inside a control loop) for restricting a frequency band of said amplitude control loop is configured by a first passive filter with lag-lead characteristics and a second passive filter of a perfect integrator type, and current-output type circuits are provided at the respective front stages of said first passive filter and said second passive filter.

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In related art, Tachimori discloses a loop filter in a control loop, which comprises filter 3 and filter 4 (paragraph [0164], Fig. 1). The examiner notices that filter 4 includes a resistor RLP and capacitor CLP. However, it is well known in the art that even without the resistor RLP (current-output type circuit), capacitor CLP itself that is being connected to the ground line would still perform as a low pass filter. Thus, the examiner interprets that resistor RF1 in series connection with capacitor CF1 is a first passive filter with lag-lead characteristic and capacitor CLP itself being connected to the ground line is a second passive filter, which is a perfect integrator type filter as defined by applicants in the abstract for including ONLY one capacitor. Also, resistor RLP is interpreted as a current-output circuit at the front stage of the second passive filter.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of Tachimori on loop filter into the teachings of Midegaard et al. for the purpose of being able to easily adjust the parameter values to meet the desired performance of the transmitter.

Consider **claim 6, as applied to claim 1 above**, Midegaard et al., as modified by Tachimori, further discloses a transmitter,

wherein a first automatic gain controlled amplifier (read as a compensation element, for example, variable gain amplifier, paragraph [0055] to [0056]) is provided on a feedback path from said power amplifier to said amplitude detector (see **Claim Rejections - 35 USC § 112** above) in said amplitude control loop path (read as the path between the output of the amplifier 33 and the input to the envelope detector 27, paragraph [0055]); a second automatic gain controlled amplifier (read as a

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compensation element, for example, variable gain amplifier, paragraph [0055] to [0056]) is provided on a forward path from *said amplitude detector* (see ***Claim Rejections - 35 USC § 112*** above) to said power amplifier in said amplitude control loop (read as the path between comparator 29 and the amplifier envelope control mechanism 31, paragraph [0055] to [0056]); The examiner interprets that circuit connection of envelope detector 27, 28 and comparator 29 as a amplitude detector.

However, Midegaard et al. failed to specifically disclose gains of said first and second automatic gain controlled amplifiers are controlled such that a product of the gain of said first automatic gain controlled amplifier and said gain of the second automatic gain controlled amplifier are kept approximately constant.

Nonetheless, applicants are reminded that in order for the automatic gain amplifiers to work, these amplifiers have to have at least one **variable** in each of them. Thus, the automatic gain amplifiers recited by applicants can also be called as variable gain amplifiers, which are taught by Midegaard et al. In addition, since these variable gain amplifiers are with variables, it would be easy for a person with ordinary skill in the art by the time of the invention to vary the variables of these amplifiers to make the product of the gains of these amplifiers to keep approximately constant.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the variable gain amplifiers taught by Midegaard et al. to obtain the same result as applicants' claimed invention because the variable within each amplifier is *variable*.

Consider **claim 7, as applied to claim 1 above**, Midegaard et al., as modified by Tachimori, further discloses a transmitter,

wherein a bias (read as the output from slow modulator 52, paragraph [0052], Fig. 7) is given such that said power amplifier is operated in nonlinear area (non-linear power amplifier) in both of the said first and second operating modes (read as slow modulator 52 sets an optimum power supply voltage for a given output power level, while the bias control arrangement 47, 48 according to the second aspect handles the envelope variation due to modulation, paragraph [0052], Fig. 7) (see ***Claim Rejections - 35 USC § 112*** above).

Consider **claim 9, as applied to claim 1 above**, Midegaard et al., as modified by Tachimori, further discloses the claimed invention and that the transmitter is for a wireless communication system (Figure1 and 2). However, Midegaard et al. fails to expressly disclose a base band circuit for generating a base band signal on the basis of transmission data, and a modulator for performing a phase modulation and an amplitude modulation in accordance with base band signal generated in said base band circuit.

Nonetheless, it is inherent that the wireless communication device of Midegaard et al. has a base band circuit to generate a base band signal on the basis of transmission data. Further, Midegaard et al. discloses a transmitter which separates the envelope and phase components of an input modulated RF signal into two separate path 19 (envelope path), 20 (phase path, paragraph [0045]). Therefore, it is inherent that there is a modulator exists in such system or apparatus to perform a phase

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modulation and an amplitude modulation in accordance with a base band signal generated in said base band circuit.

Therefore, claim 9 is rejected for claiming inherent subject matters.

**Claims 3-5** are rejected under 35. U.S.C. 103(a) as being unpatentable over **Midtgaard et al. (U.S. PGPub 2002/0090921 A1)** in view of **Tachimori (U.S. PGPub 2002/0051508 A1)** as applied to claim 1 above, and in further view of **Tsutsui et al. (U.S. PGPub 20050218989)**.

Consider **claim 3, as applied to claim 1 above**, Midtgaard et al. in view of Tachimori discloses the claimed invention but does not disclose expressly a transmitter, wherein in a first operating mode a phase and amplitude modulation by said phase control loop and said amplitude control loop is performed to transmit a signal; in a second operating mode, a phase modulation by said phase control loop is performed to transmit a signal; and in said first operating mode and said second operating mode said phase control loop is in common used to perform a phase modulation.

In related art, Tsutsui et al. discloses a transmitter (read as the transmitter in a wireless communication system, abstract), wherein in a first operating mode a phase and amplitude modulation by said phase control loop and said amplitude control loop is performed to transmit a signal (read as in EDGE mode transmission, the high frequency implements the 8-PSK modulation for rendering phase shift and amplitude shift, paragraph [0037]); in a second operating mode, a phase modulation by said phase control loop is performed to transmit a signal (read as in GSM mode transmission 8-PSK, the high frequency implements the GMSK modulation for rendering phase

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modulation, paragraph [0037]); and in said first operating mode (read as EDGE mode transmission, abstract) and said second operating mode (read as GMSK mode transmission) said phase control loop (read as the phase control loop exists in the transmitter of the transmission system) is in common used to perform a phase modulation.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of Tsutsui et al. into the teachings of Midtgaard et al. in view of Tachimori to allow the transmitter in a wireless transmission system to perform dual mode modulation.

Consider **claim 4, as applied to claim 3 above**, Midtgaard et al., as modified by Tachimori and Tsutsui et al., discloses the claimed invention but does not disclose the transmitter, wherein said first passive filter is provided at a front stage thereof prior to said second passive filter.

Nonetheless, Tachimori further discloses first passive filter (read as Lag-Lead filter that includes RF1 and CF1, Fig. 1) is provided at a front stage thereof prior to said second passive filter (read as the low pass filter that include ONLY a capacitor CLP, Fig. 1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to further incorporate the teaching of Tanchimori into the teachings of Midtgaard et al., which modified by Tanchimori and further modified by Tsutsiu et al. to provide a second passive filter after the first passive filter for the purpose of reducing the influence of noise.

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Consider **claim 5, as applied to claim 4 above**, Midtgaard et al., as modified by Tachimori and Tsutsui et al., discloses the claimed invention with a circuit provided at a rear stage of said second passive filter (read as Envelope controller 31, Fig. 5) but does not expressly disclose the transmitter, wherein said current-output type circuit provided at a front stage of said second passive filter is designed to configure a perfect integrator circuit comprising said current-output type circuit, said second passive filter, and a circuit provided at a rear stage of said second passive filter.

Nonetheless, Tachimori discloses a loop filter that comprises a current-output type circuit (read as resistor RLP, Fig. 1), said second passive filter (read as capacitor CLP, Fig. 1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to further incorporate the teaching of Tanchimori into the teachings of Midtgaard et al., which modified by Tanchimori and further modified by Tsutsiu et al. to configure a perfect integrator circuit comprising said current-output type circuit (read as resistor RLP, Fig. 1), said second passive filter (read as capacitor CLP, Fig. 1), and a circuit provided at a rear stage (read as Envelope controller 31, Fig. 5) of said second passive filter for the purpose of increasing the signal-to-noise ratio.

**Claim 8** is rejected under 35. U.S.C. 103(a) as being unpatentable over **Midtgaard et al. (U.S. PGPub 2002/0090921 A1)** in view of **Tachimori (U.S. PGPub 2002/0051508 A1)** as applied to **claim 1 above**, and in further view of **Horii et al. (U.S. Patent 5,715,527)**.



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Consider **claim 8, as applied to claim 1 above**, Midtgaard et al., as modified by Tachimori, discloses the claimed invention but fails to disclose a transmitter, wherein said power amplifier is configured by a field effect transistor, and a voltage generated in said amplitude control loop is applied to one of a drain and a source of said field effect transistor to control a gain of said transistor.

In related art, Horii et al. discloses a power amplifier (read as power amplifier 11, column 5 lines 50-54, Fig. 1) comprises an FET (Field-Effect Transistor), and a generated voltage in an amplitude control loop is applied to one of a drain and a source of said field effect transistor to control a gain of said transistor (read as gain control signal 181 applied to the drain of the FET to increase the gain of the FET, column 5, lines 50-55, Fig. 1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teaching of Horii et al. into the teachings of Midtgaard et al., which modified by Tachimori for the advantage that FET type power amplifier can be easily integrated.

**Claim 10** is rejected under 35. U.S.C. 103(a) as being unpatentable over **Midtgaard et al. (U.S. PGPub 2002/0090921 A1)** in view of **Tachimori (U.S. PGPub 2002/0051508 A1)** as applied to **claim 9 above**, and in further view of **Duperray (U.S. PGPub 2003/0095608 A1)**.

Consider **claim 10, as applied to claim 9 above**, Midtgaard et al., as modified by Tachimori, discloses the claimed invention but fails to disclose a wireless communication apparatus wherein a signal for controlling a gain of said first automatic

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gain control amplifier and a gain of said second automatic gain controlled amplifier is generated in said base band circuit.

In related art, Duperray discloses the signals (read as C1, C2, C3, paragraph [26] Fig. 1) for controlling the gains of variable gain controlled amplifiers (read as variable gain power amplifier 9 and 17, paragraph [26], Fig. 1) are generated in base band circuit (read as base band unit 20, paragraph [26], Fig. 1)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teaching of Duperray into the teachings of Midtgaard et al., as modified by Tachimori to control the gains of automatic gain control amplifiers so the output of the automatic gain control amplifiers will have a desired relationship between them because the gain control signals are from the same source.

### ***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sparks	(U.S. Patent 5,469,105)	Transmitter and power amplifier therefor
Tsutsui et al.	(U.S. Patent 6,636,114 B2)	High frequency power amplifier module and wireless communication apparatus
Cordoba	(U.S. Patent 6,671,337 B1)	Carrier modulator for use in a transmitter or transceiver
Hayashihara	(U.S. Patent 6,766,156 B1)	Radio transmitter-receiver, high-frequency radio receiver, and control

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unit

Rozenblit et al.	(U.S. Patent 6,801,784 B1)	Continuous closed-loop power control system including modulation injection in a wireless transceiver power amplifier
Asam et al.	(U.S. Patent 6,853,836 B2)	Polar loop transmission circuit

9. Any response to this Office Action should be **faxed to (571) 273-8300 or mailed to:**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**Hand-delivered responses** should be brought to

Customer Service Window  
Randolph Building  
401 Dulany Street  
Alexandria, VA 22314

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junpeng Chen whose telephone number is (571) 270-1112. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

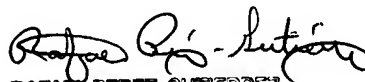
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rafael Perez-Gutierrez can be reached on 571-272-7915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Junpeng Chen  
J.C./jc

May 15, 2006

  
RAFAEL PEREZ-GUTIERREZ  
PRIMARY EXAMINER  
5/24/06